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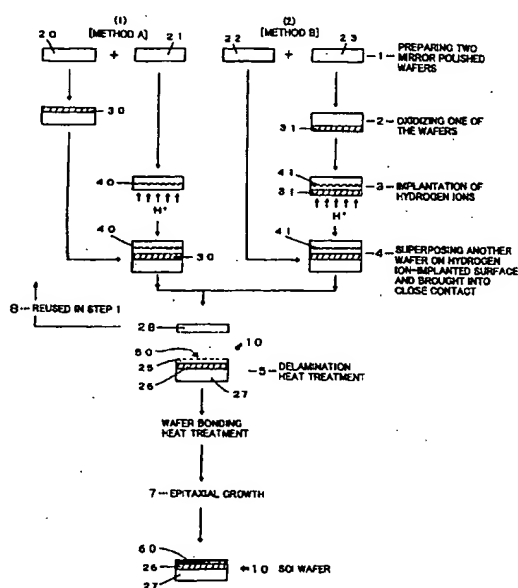
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(54) "A method of fabricating an SOI wafer and SOI wafer fabricated by the method"

(57) There is disclosed a method of fabricating an SOI wafer characterized in that an oxide film is formed on at least one of two single crystal silicon wafers; hydrogen ions or rare gas ions are implanted into the upper surface of one of the two silicon wafers in order to form an ion implanted layer; the ion-implanted surface is brought into close contact with the surface of the other silicon wafer via the oxide film; heat treatment is performed to separate a thin film from the silicon wafer with using the ion implanted layer as a delaminating plane to fabricate the SOI wafer having an SOI layer; and then an epitaxial layer is grown on the SOI layer to form a thick SOI layer. There is provided an SOI wafer which has a thick SOI layer with good thickness uniformity and good crystallinity and which is useful for a bipolar device or a power device.

FIG. 1



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## Description

### BACKGROUND OF THE INVENTION

#### Field of the Invention:

[0001] The present invention relates to a method of increasing thickness of an SOI (silicon on insulator) layer in an SOI structure wafer obtained by a method wherein an ion-implanted wafer is bonded to another wafer and a portion of the ion-implanted wafer is delaminated to provide an SOI wafer (the technique called a hydrogen ion delamination method, or a smart-cut method), and an SOI wafer produced by the method.

#### Description of the Related Art:

[0002] One of typical method for producing an SOI wafer is a so-called wafer bonding method in which two mirror-polished silicon wafers are bonded together via an oxide film without use of adhesive, then subjected to a heat treatment (generally 1000°C to 1200°C) to increase a bonding strength, and one of the wafers is subsequently made thin.

[0003] In the wafer bonding method, thickness of one of the two wafers which are bonded to each other is made thin with grinding or etching to some extent, and then the surface thereof is subjected to a mechanochemical polishing to be finished to have an intended thickness of the SOI layer.

[0004] The SOI wafer fabricated according to the method has an advantage that crystallinity of the SOI layer and reliability of a buried oxide layer are as high as those of general silicon wafers. However, it has a disadvantage that thickness uniformity of the SOI layer achieved in the method is limited. Namely, only the uniformity in the surface of the intended thickness  $\pm 0.3 \mu\text{m}$  can be achieved even if a highly precise processing method is used. Furthermore, there exists a problem of high production cost, since only one SOI wafer can be obtained from two silicon wafers.

[0005] Recently, a new method of fabricating an SOI wafer in which an ion-implanted wafer is bonded to another wafer and the wafers are then subjected to a heat treatment to be delaminated at an ion implanted layer (the technique called a hydrogen ion delamination method, or a smart-cut method) has been proposed in Japanese Patent Application Laid-Open (kokai) No. 5-211128. In this method, an oxide film is formed on the surface of at least one of two silicon wafers; hydrogen ions or rare gas ions are implanted into one surface of one of the two silicon wafers in order to form a fine bubble layer (enclosed layer) within the wafer; the ion-implanted silicon wafer is superposed on the other silicon wafer such that the ion-implanted surface comes into close contact with the surface of the other silicon wafer via the oxide film; heat treatment at 500°C or more is then performed to delaminate a portion of the ion-im-

planted wafer with using the fine bubble layer as a delaminating plane, so as to delaminate a thin film; and heat treatment at high temperature is further performed to firmly bond the wafers to each other, to thereby obtain an SOI wafer. According to the method, the SOI wafer having a thickness uniformity of  $\pm 0.01 \mu\text{m}$  or less can be fabricated relatively easily.

[0006] A so-called thick layer SOI wafer which has a SOI layer having a thickness of several microns to tens microns is very useful for a bipolar device or a power device, and further development thereof is greatly expected.

[0007] The thick layer SOI wafer has been conventionally fabricated by the above-mentioned wafer bonding method, namely, by bonding a wafer having an oxide film and a bare wafer to each other, subjecting them to a bonding heat treatment at 1100°C, and grinding and polishing them to provide a thick layer SOI wafer having a desired thickness. In the method, since the wafers are not bonded to each other in the peripheral part, it is necessary to perform an edge treatment step for removing the unbonded portion before polishing. Such a step makes the method complicate, and increases production cost. Furthermore, it is not possible to improve thickness uniformity of the SOI layer only by a polishing process, and therefore, a vapor phase etching treatment called PACE (Plasma Assisted Chemical Etching) disclosed in Japanese Patent Application Laid-Open (kokai) No. 5-160074 has been performed to make thickness uniform, and the mirror polishing has been performed to remove hazes or the like. When polishing is performed after the vapor phase etching as described above, thickness uniformity of the SOI layer may be rather deteriorated, latent flaws or a damage layer may be incorporated, and crystallinity may be lowered. Furthermore, processing cost is high also in that case.

[0008] On the other hand, the hydrogen ion delamination method are significantly advantageous in productivity and cost performance, since the edge treatment process which is essential in the above-mentioned wafer bonding method is not necessary.

[0009] However, only an SOI layer having a thickness of  $2 \mu\text{m}$  at most can be produced by the method, since the thickness of the SOI layer depends on a depth of ion implantation, which depends on an acceleration voltage of an ion implanter, and only about 200 keV of acceleration voltage at most is possible in high current ion implanter generally used for mass-production, because of limitation in the apparatus.

[0010] Accordingly, in order to form a thicker SOI layer by the hydrogen ion delamination method, the high current ion implanter which can provide a higher acceleration voltage is necessary. However, when the apparatus which can provide high acceleration voltage more than 200 keV is used, it takes long time to achieve a certain amount of ion implantation and thus cost is increased, since it is difficult to obtain high current by such an apparatus. Therefore, such an apparatus has not been

used in mass-production. Furthermore, as in a PACE method, there is also a problem that a process such as polishing or the like is necessary in order to improve a surface roughness on the surface of SOI after delamination.

#### SUMMARY OF THE INVENTION

**[0011]** The present invention has been accomplished to solve the above-mentioned problems, and a major object of the present invention is to provide a method of fabricating a thick layer SOI wafer having excellent thickness uniformity in high productivity and at low cost by forming a silicon film on an SOI wafer obtained by hydrogen ion delamination method.

**[0012]** To achieve the above mentioned object, the present invention provides a method of fabricating an SOI wafer characterized in that an oxide film is formed on at least one of two single crystal silicon wafers; hydrogen ions or rare gas ions are implanted into the upper surface of one of the two silicon wafers in order to form an ion implanted layer; the ion-implanted surface is brought into close contact with the surface of the other silicon wafer via the oxide film; heat treatment is performed to separate a thin film from the silicon wafer with using the ion implanted layer as a delaminating plane to fabricate the SOI wafer having an SOI layer; and then an epitaxial layer is grown on the SOI layer to form a thick SOI layer.

**[0013]** As described above, when the epitaxial layer is grown on the SOI layer without polishing delaminating plane of the SOI layer after the SOI wafer having the SOI layer is obtained by the hydrogen ion delamination method, the thick layer SOI wafer having a good thickness uniformity can be fabricated in good yield and in high productivity. Furthermore, since the SOI wafer is exposed to hydrogen atmosphere while the temperature is increased before epitaxial growth to thereby improve surface roughness of the surface of the SOI layer, surface roughness of the thick layer SOI wafer after growth of the epitaxial layer can also be improved.

**[0014]** In that case, since the epitaxial layer is formed on the delaminated surface of the SOI layer that still include a damage layer caused by ion implantation in some degree, the thick layer SOI wafer having the damage layer in the SOI layer under the epitaxial layer can be fabricated. In the wafer, the damage layer can be used as a gettering site for removing impurities such as heavy metal from the device active layer.

**[0015]** When the SOI wafer before epitaxial growth is subjected to a heat treatment in a reducing atmosphere including hydrogen or in an atmosphere including hydrogen chloride gas, a damage layer remaining on the delaminated surface of SOI layer can be removed, so that the epitaxial layer can be grown on the delaminated surface whose surface roughness has been improved. As a result, an SOI wafer that contains very few crystal defects and has a thick SOI layer with high quality such

as good thickness uniformity and surface roughness can be fabricated.

**[0016]** When the SOI wafer is fabricated using the silicon wafer produced by Czochralski method (CZ method), void type defects having a size of 0.1 to 0.2  $\mu\text{m}$ , called COP (Crystal Originated Particle), are present in the SOI layer. Accordingly, if the thickness of the SOI layer is thinner than the size of COP, hydrogen gas used in the epitaxial growth process passes through the COP, and etches the buried oxide layer, resulting in degradation of characteristics of SOI wafer.

**[0017]** Accordingly, the thickness of the SOI layer of the SOI wafer before growth of the epitaxial layer is preferably 0.2  $\mu\text{m}$  or more, to surely prevent the buried oxide layer from being etched during the epitaxial growth process.

**[0018]** The thickness of the thick SOI layer after epitaxial growth is preferably more than 2  $\mu\text{m}$ .

**[0019]** When the thick SOI layer is formed as described above, the thick SOI layer which is quite useful for a bipolar device or a power device and has good thickness uniformity can be fabricated in high productivity and with good cost performance.

**[0020]** The present invention also provides an SOI wafer fabricated by the method described above.

**[0021]** Such an SOI wafer is excellent in thickness uniformity and electric characteristics, and therefore is quite useful for a bipolar device or a power device.

**[0022]** The present invention also provides a method for reusing a delaminated wafer produced as a by-product in the methods described above as a silicon wafer by reprocessing it.

**[0023]** According to the method, a delaminated wafer produced as a by-product in the hydrogen ion delamination method of the present invention can also be reused as a silicon wafer after being reprocessed appropriately, and as a result, yield and productivity of the SOI wafer which has a thick SOI layer with good quality can be improved, and cost reduction can be achieved.

**[0024]** As described above, according to the present invention, an SOI wafer having a thick SOI layer excellent in thickness uniformity, crystallinity and electric characteristics, which is useful as a bipolar device or a power device, or an SOI wafer having a gettering site in the SOI layer and having a strong resistance to heavy metal contamination can be fabricated relatively easily at low cost.

**[0025]** Furthermore, in the method of the present invention, neither a process for making a film thin nor a polishing process for improving surface roughness is necessary, and therefore amounts of water to be used and industrial wastes such as polishing slurry are reduced, and thus, harmful influence on environment can be prevented. Furthermore, since a process for removing the unbonded part in the periphery of the wafer is not necessary, productivity and yield are further improved, enabling drastic cost reduction. Recycle of the delaminated wafer produced as a by product as a silicon

wafer may further reduce the cost.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0026] Fig.1 is a flowchart showing an example of an SOI-wafer fabricating process of the present invention.

#### DESCRIPTION OF THE INVENTION AND A PREFERRED EMBODIMENT

[0027] The present invention will be further described below in detail, referring a figure, but is not limited thereto.

[0028] Fig.1 is a flowchart showing an example of an SOI wafer fabricating process including an epitaxial growth process, in which an ion-implanted wafer is bonded to another wafer and a portion of the ion-implanted wafer is delaminated to thereby fabricate an SOI wafer.

[0029] The hydrogen ion delamination method can be performed in two different ways, namely Method A and Method B which are different from each other in the sequence of process steps. First, a method of fabricating SOI wafer having thick film of the present invention according to Method A will be described.

[0030] In Step 1 of Method A as shown in Fig.1 (1), two silicon mirror wafers 20, 21 which are suitable for device specifications are prepared.

[0031] In Step 2, at least one of the wafers (the wafer 20 in this case) is subjected to thermal oxidation so as to form on the surface thereof an oxide film 30 having a thickness of about 0.1  $\mu\text{m}$  to 2.0  $\mu\text{m}$ . In the figure, the oxide film is formed only on one surface. However, the oxide film may be formed all over the surface of the wafer 20.

[0032] In Step 3, hydrogen ions or rare gas ions are implanted into one surface of the other wafer 21, in order to form a fine bubble layer (enclosed layer) 40 which lies in parallel to the surface at a position corresponding to the mean depth of ion implantation. The implantation temperature is preferably 25 - 450°C.

[0033] Depth of implantation of ions depends on acceleration voltage of an ion implanter, and the thickness of SOI layer after delamination depends on the depth of implantation of ions. However, there is a limit to acceleration voltage of the ion implanter. The acceleration voltage of about 200 keV, which means thickness of about 2  $\mu\text{m}$ , for example, in the case of hydrogen ion implantation, is upper limit at present.

[0034] In Step 4, the wafer 20 is superposed on the hydrogen ion-implanted surface of the hydrogen ion-implanted wafer 21 via the oxide film 30, and they are brought in close contact with each other. When the surfaces of the two wafers are brought into contact with each other at ambient temperature in a clean atmosphere, the wafers are bonded to each other without use of adhesive or the like.

[0035] In Step 5, there is performed a heat treatment

for delamination in which the upper silicon (a delamination wafer) 28 is delaminated from the lower SOI wafer 10 (composed of the SOI layer 25, a buried oxide layer 26, and a base wafer 27) at the enclosed layer 40. The heat treatment is performed at a temperature of about 500°C or higher in an inert gas atmosphere so as to cause crystal rearrangement and bubble cohesion, and thereby the delamination wafer 28 is delaminated (separated) from the lower SOI wafer. As described above, the delaminated wafer 28 is produced as a by-product in Step 5 in the present invention.

[0036] In Step 6, the wafers which have been bonded to each other in the above-mentioned Step 4, the bonding step, are subjected to heat treatment in order to improve bonding strength to a sufficient level, since the bonding strength imparted in Step 4 is too low for use in a device process. Preferably, this heat treatment is performed in an inert gas atmosphere or an oxidizing gas atmosphere at 1050 - 1200°C for 30 minutes to 2 hours.

[0037] The heat treatment for delamination in Step 5 and the heat treatment for bonding in Step 6 as mentioned above may be successively performed. Alternatively, a single heat treatment serving as both of Steps 5 and 6 may be performed. The steps described above are the same as the steps of the method for fabricating an SOI wafer according to a general hydrogen ion delamination method.

[0038] In Step 7, the epitaxial layer is grown on the delaminated surface 50 which is a surface of the SOI layer 25 obtained by a hydrogen ion delamination method in order to increase a thickness of the SOI layer to a desired thickness which is more than 2  $\mu\text{m}$ .

[0039] In Method A, since there is a region (non bonding portion) where an oxide film 30 (buried oxide layer 26) is exposed in the peripheral part of SOI wafer 10 after the delamination heat treatment, it is necessary to remove it in advance with an aqueous solution of hydrofluoric acid or the like before epitaxial growth. The SOI wafer 10 finally obtained after epitaxial layer growth consists of a thick SOI layer 60 having a total thickness of several microns to several tens microns, a buried oxide layer 26 and a base wafer 27.

[0040] Epitaxial growth may be performed according to CVD method as generally performed, for example, by reducing  $\text{SiCl}_4$ ,  $\text{SiHCl}_3$ ,  $\text{SiH}_2\text{Cl}_2$ ,  $\text{SiH}_4$  or the like with hydrogen at 1100 - 1200°C, to precipitate Si so that epitaxial growth may be obtained in the same crystal orientation as that of the used silicon wafer.

[0041] Alternatively, epitaxial growth can also be performed according to a molecular beam epitaxy method (MBE method) under super high vacuum ( $10^{-8}$  to  $10^{-11}$  Torr), at low temperature as 600 to 900°C.

[0042] The sequence of the above-mentioned steps, namely the Steps 5-6-7 may be changed to the Steps 5-7-6.

[0043] The bonding heat treatment of Step 6 and epitaxial growth of Step 7 can also be performed succes-

sively, or the treatment serving as both of Step 6 and Step 7 can also be performed.

[0044] For example, a general epitaxial growing process comprises providing a reactant gas to deposit an epitaxial layer after increasing temperature to 1000 to 1200 °C in 100 % hydrogen atmosphere. Even only the above-mentioned process can improve bonding strength with epitaxial growth. Alternatively, a damage layer on the surface of the SOI is etched by being kept in an atmosphere of hydrogen or a mixed atmosphere of hydrogen chloride gas and hydrogen for a predetermined period after increasing the temperature around a reaction temperature, and then the deposition of the epitaxial layer can be successively performed. In that case, bonding strength can also be improved as a result.

[0045] Step 6 and Step 7 can be performed successively or at the same time in the same epitaxial apparatus in the above method, and thus the method is very advantageous in productivity and cost performance.

[0046] As described above, when epitaxial growth of silicon is performed on the delaminated surface of the SOI layer obtained by the hydrogen ion delamination method, the thick SOI layer having a total thickness of several microns to several tens microns can be obtained relatively easily, and an SOI wafer having uniform thickness, containing almost no crystal defects, and excellent in electric characteristics, or an SOI wafer having a gettering site in the SOI layer and having a resistibility to heavy metal contamination can be fabricated.

[0047] Next will be described a method of fabricating SOI wafer according to Method B. In Step 1 of Method B, there are prepared two mirror silicon wafers 22 and 23 suitable for device specifications.

[0048] In Step 2, at least one of the wafers is subjected to thermal oxidation to form on the surface thereof an oxide film 31 having a thickness of about 0.1 - 2.0 µm.

[0049] In Step 3, hydrogen ions or rare gas ions are implanted into the oxide film 31 of the wafer 23 in order to form a fine bubble layer (enclosed layer) 41 which lies in parallel to the surface at a position corresponding to the mean depth of ion implantation. The implantation temperature is preferably 25 - 450°C.

[0050] In Step 4, the silicon wafer 22 is superposed on the surface of the oxide film 31, which is the surface to which hydrogen ions have been implanted, of the ion-implanted wafer 23. When the surface of the two wafers are brought into contact with each other at ambient temperature in a clean atmosphere, the wafers are bonded to each other without use of adhesive or the like.

[0051] Subsequently, in Steps 5 to 7, the same treatment processes as those in Method A are performed, to thereby obtain an SOI wafer which has a thick SOI layer having uniform thickness without crystal defects.

[0052] Step 8 in this method is a step for reusing a delaminated wafer. In this step, the delaminated wafer 28 produced as a by-product in the Step 5, which is a step of the heat treatment for delamination, is reused as a silicon wafer. The wafers produced as a by-product in

either Method A or Method B can be reused.

[0053] The step for reusing is designed suitably depending on the quality of the delaminated wafer. For example, when a step due to an unbonded portion and an oxide film or a damage layer remains in the peripheral part of the delaminated wafer, the reusing step includes a polishing process for polishing the delaminated surface.

[0054] The heat treatment in a reducing atmosphere including hydrogen can also be performed to remove the damage layer on the surface and improve the surface roughness.

[Examples]

[0055] The following examples are being submitted to further explain the present invention. These examples are not intended to limit the scope of the present invention.

(Example 1)

[0056] Two CZ silicon mirror wafers of conductive type p having a resistivity of 10 Ω-cm, a diameter of 150 mm and crystal axis of <100> were prepared. These wafers were processed through Steps 1 to 8 of Method B shown in Fig. 1 to thereby obtain SOI wafers according to the hydrogen ion delamination method, which have an SOI layer having a thickness of 0.5 µm, and then an epitaxial layer is grown by CVD method to produce SOI wafers which have a thick SOI layer having a total thickness of 2.0 µm.

[0057] The major process conditions for fabricating SOI wafers were as follows.

- a) Thickness of the oxide film in Step 2: 80 nm;
- b) Condition of hydrogen implantation in Step 3: H<sup>+</sup> ions, implantation energy: 67 keV, implantation dose:  $8 \times 10^{16}/\text{cm}^2$ ;
- c) Conditions of heat treatment for delamination in Step 5: in a N<sub>2</sub> gas atmosphere, at 500°C for 30 minutes;
- d) Bonding heat treatment of Step 6: none (Step 7 serves also as it);
- e) Conditions of epitaxial growth by CVD method in Step 7: H<sub>2</sub> bake (H<sub>2</sub> atmosphere, 1110°C, 60 seconds), epitaxial layer deposition (SiHCl<sub>3</sub> + H<sub>2</sub>, 1110°C, 60 seconds).

[0058] An SOI layer having a thickness of 0.5 µm was formed according to the hydrogen ion delamination method in Step 5, and a thick SOI layer having a total thickness of 2.0 µm was formed by performing epitaxial growth of 1.5 µm according to the CVD method in Step 7.

[0059] Thickness uniformity and surface roughness of the SOI layer of the SOI wafer just delaminated after the heat treatment for delamination of Step 5 was measured. Thickness was measured by the spectral reflect-

ance measurement at several thousands points in 2 mm pitch on the surface area other than the area within 10 mm from the periphery of the SOI wafer, and the results were indicated in RMS value (root-mean-square value). According to the results, a sigma (standard deviation) of the thickness of the SOI layer after the delamination heat treatment was 0.6 nm, and therefore thickness uniformity (3 sigma) was  $\pm 1.8$  nm. Surface roughness was measured by an atomic force microscope over a measuring area of 1  $\mu\text{m}$  square, and it was expressed in the RMS value (root-mean-square roughness) as about 7.6 nm.

[0060] On the other hand, thickness distribution of the SOI layer after epitaxial growth in Step 7 was measured. A sigma (standard deviation) of the thickness was 18.4 nm, and therefore thickness uniformity (3 sigma) was  $\pm 55.4$  nm. From the results, it is apparent that thickness uniformity was lowered little by the epitaxial growth, but was still quite excellent compared with the value,  $\pm 0.3$   $\mu\text{m}$ , of the wafer fabricated by a general wafer bonding method. Surface roughness was Rms value of about 0.29 nm and quite excellent.

[0061] The SOI wafer was divided into four pieces after the epitaxial growth, and a defect density in the depth direction of the SOI layer was measured. The four pieces of the wafer were etched with KOH aqueous solution at a etching removal of 1.5, 1.0, 0.5, 0  $\mu\text{m}$  from the surface. The pieces were then subjected to the four step Secco etching method disclosed in H. Gassel et al. (J. Electrochem. Soc., 140, pp1713, 1993), and observed with a microscope to count a density of pits existing on the surface.

[0062] The defect density was  $10^2/\text{cm}^2$  or less at any depth, which was equal to or less than that of a general bulk wafer, and was quite excellent.

#### [Example 2]

[0063] An SOI wafer having a total thickness of 7.0  $\mu\text{m}$  was fabricated in the same manner as Example 1 except that thickness achieved by epitaxial growth was 6.5  $\mu\text{m}$  and an epitaxial layer was deposited without  $\text{H}_2$  bake (the heat treatment in approximately 100 % hydrogen atmosphere). Surface roughness expressed in the RMS value was quite excellent as about 0.33 nm.

[0064] The SOI wafer was divided into four pieces. One of them was subjected to a general preferential etching (Secco etching) at an etching removal of 1  $\mu\text{m}$ , and observed with a microscope to measure the defect density on the surface. No defect such as stacking fault was observed.

[0065] The other three of them were evaluated as for the defect density in the depth direction of the SOI layer in the same manner as Example 1 except that the etching removal with an aqueous solution of KOH was 5.0, 6.0 or 6.5  $\mu\text{m}$  from the surface of each piece.

[0066] As for the two of them in which the etching removal was 5.0, 6.0  $\mu\text{m}$  respectively, the defect density

was  $10^2/\text{cm}^2$  or less, as well as Example 1. As for the wafer in which the etching removal was 6.5  $\mu\text{m}$  (etching to a position at which epitaxial layer had began to grow), the defect density was  $7 \times 10^3/\text{cm}^2$ . The results showed that the SOI layer under the epitaxial layer still included a damage that was generated when hydrogen ion was implanted. The damage layer can be used as a gettering site for removing impurity such as heavy metals from the device active layer.

[0067] The present invention is not limited to the above-described embodiment. The above-described embodiment is a mere example, and those having substantially the same structure as that described in the appended claims and providing the similar action and effects are all included in the scope of the present invention.

#### Claims

1. A method of fabricating an SOI wafer characterized in that an oxide film is formed on at least one of two single crystal silicon wafers; hydrogen ions or rare gas ions are implanted into the upper surface of one of the two silicon wafers in order to form an ion implanted layer; the ion-implanted surface is brought into close contact with the surface of the other silicon wafer via the oxide film; heat treatment is performed to separate a thin film from the silicon wafer with using the ion implanted layer as a delaminating plane to fabricate the SOI wafer having an SOI layer; and then an epitaxial layer is grown on the SOI layer to form a thick SOI layer.
2. The method of fabricating an SOI wafer according to Claim 1 characterized in that the SOI wafer before the growth of the epitaxial layer is subjected to a heat treatment in a reducing atmosphere including hydrogen or in an atmosphere including hydrogen chloride gas.
3. The method of fabricating an SOI wafer according to Claim 1 or 2 characterized in that the thickness of the SOI layer of the SOI wafer before the growth of the epitaxial layer is 0.2  $\mu\text{m}$  or more.
4. The method of fabricating an SOI wafer according to any one of Claims 1 to 3 characterized in that the thickness of the thick SOI layer after the epitaxial growth is 2  $\mu\text{m}$  or more.
5. An SOI wafer fabricated by the method according to any one of Claims 1 to 4.
6. A method for reusing a delaminated wafer produced as a by-product in the method according to any one of Claims 1 to 4 as a silicon wafer after reprocessing it.

7. A thick layer SOI wafer fabricated by growing an epitaxial layer on an SOI layer characterized in that a damage layer is present in the SOI layer under the epitaxial layer.

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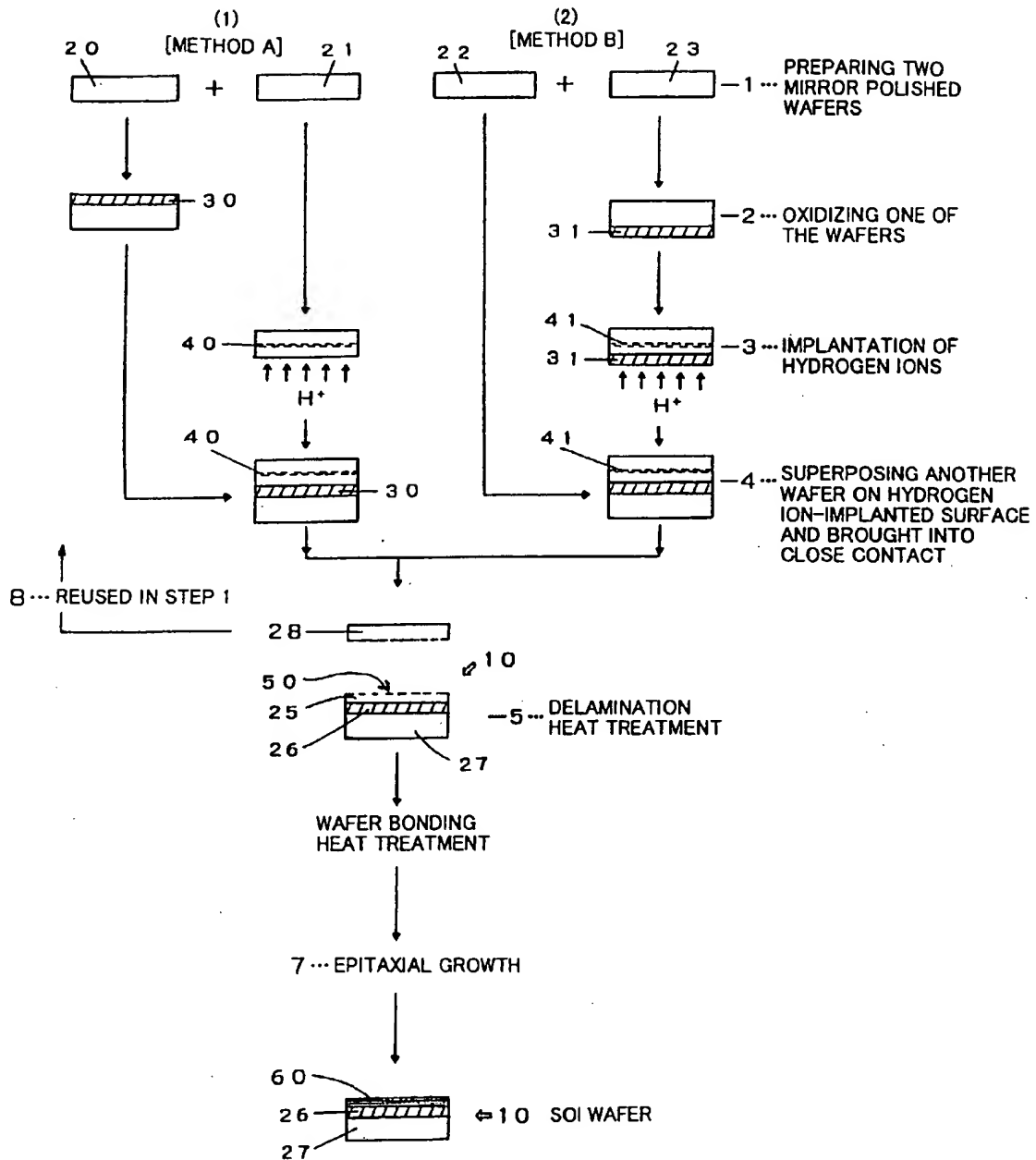
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FIG. 1







European Patent  
Office

# EUROPEAN SEARCH REPORT

Application Number  
EP 99 30 5120

| DOCUMENTS CONSIDERED TO BE RELEVANT   |   |  |  |
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| Place of search<br><b>THE HAGUE</b>   |   | Date of completion of the search<br><b>29 October 1999</b> | Examiner<br><b>Wirner, C</b>                 |
| CATEGORY OF CITED DOCUMENTS<br>X: particularly relevant if taken alone<br>Y: particularly relevant if combined with another document of the same category<br>A: technological background<br>O: non-written disclosure<br>P: intermediate document<br>T: theory or principle underlying the invention<br>E: earlier patent document, but published on, or after the filing date<br>D: document cited in the application<br>L: document cited for other reasons<br>& : member of the same patent family, corresponding document |   |  |  |

EPO FORM 1503 (04.98) (mod.01)



European Patent  
Office

# EUROPEAN SEARCH REPORT

Application Number  
EP 99 30 5120

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| Category   | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim  | CLASSIFICATION OF THE APPLICATION (Int. CL.7) |
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|  |   |  | TECHNICAL FIELDS SEARCHED (Int. CL.7)         |
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| The present search report has been drawn up for all claims   |   |  |   |
| Place of search<br><b>THE HAGUE</b>  |   | Date of completion of the search<br><b>29 October 1999</b> | Examiner<br><b>Wirner, C</b>                  |
| <p><b>CATEGORY OF CITED DOCUMENTS</b></p> <p>X : particularly relevant if taken alone<br/> Y : particularly relevant if combined with another document of the same category<br/> A : technological background<br/> O : non-written disclosure<br/> P : intermediate document</p> <p>T : theory or principle underlying the invention<br/> E : earlier patent document, but published on, or after the filing date<br/> D : document cited in the application<br/> L : document cited for other reasons</p> <p>&amp; : member of the same patent family, corresponding document</p> |   |  |   |

EPO FORM 1605 (03/92) (P04001)

**ANNEX TO THE EUROPEAN SEARCH REPORT  
ON EUROPEAN PATENT APPLICATION NO.**

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This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on  
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